This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1. - 20. (Cancelled)

21. (Currently Amended) A method comprising:

locking a resource to be accessed by speculative execution of a first instruction in an instruction pipeline; and

determining, after said locking, whether a read-after-write hazard exists between an accessing portion of the first instruction, when executed in said instruction pipeline, and a portion of a second instruction based, at least in part, on order of the first instruction with respect to the second instruction as indicated in a read-after-write hazard field for said first instruction in a buffer of a load/store unit of a processor including said instruction pipeline wherein each bit in said read-after-write hazard field corresponds to an entry in a store buffer.

22. (Previously Presented) The method of claim 21 wherein the locking is performed prior to the first instruction entering a trap stage of said instruction pipeline.

23. (Previously Presented) The method of claim 21 wherein the first instruction is an atomic instruction including a portion to lock the resource and a portion to unlock the resource.

24. (Cancelled)

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25. (Previously Presented) The method of claim 21 wherein the locking includes:

locking the resource during an effective address calculation stage of said instruction pipeline.

26. (Previously Presented) The method of claim 21 wherein the locking includes locking at least a portion of a cache.

27. (Previously Presented) The method of claim 21 wherein the locking includes locking at least one memory address.

28. (Previously Presented) The method of claim 21 further comprising unlocking the resource no later than a time at which the first instruction exits said instruction pipeline, regardless of whether the first instruction is cancelled.

29. (Previously Presented) The method of claim 28 wherein said unlocking the resource includes:

unlocking the resource in the normal course of executing the first instruction.

30. (Previously Presented) The method of claim 28 wherein said unlocking the resource includes:

preventing a write portion of the first instruction from altering information held in at least a portion of the resource.

31. (Previously Presented) The method of claim 30 wherein said preventing a write portion from altering information includes suppressing writing a value to an architectural storage location.

32. (Previously Presented) A processor comprising:

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at least one processing core to lock a resource in response to speculative execution of an access portion of a first instruction in a pipeline of said processing core prior to determining whether a read-after-write hazard exists between the access portion and a portion of a second instruction based, at least in part, on order of the first instruction with respect to the second instruction as indicated in a read-after-write hazard field for said first instruction in a buffer of a load/store unit of said processor wherein each bit in said read-after-write hazard field corresponds to an entry in a store buffer.

33. (Previously Presented) The processor of claim 32 further comprising a plurality of processing cores, wherein respective processing cores are adapted to lock the resource in response to respective accesses by respective first instructions prior to determining whether said read-after-write hazard exists between the respective accesses and the second instruction.

34. (Previously Presented) The processor of claim 32 wherein said at least one processing core is adapted to lock the resource prior to the first instruction entering a trap stage of said pipeline.

35. (Previously Presented) The processor of claim 32 wherein said at least one processing core is adapted to implement an atomic instruction, wherein implementing the atomic instruction includes locking the resource and unlocking the resource.

36. (Cancelled)

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37. (Previously Presented) The processor of claim 32 wherein said at least one processing core is adapted to lock the resource during an effective address calculation stage of said pipeline.

38. (Previously Presented) The processor of claim 32 further including a cache, and wherein said at least one processing core is adapted to lock at least a portion of the cache.

39. (Previously Presented) The processor of claim 32 wherein said at least one processing core further includes an output coupled to a memory, and wherein said at least one processing core is adapted to lock at least one memory address.

40. (Previously Presented) The processor of claim 32 further comprising logic to unlock the resource no later than a time at which the first instruction exits said pipeline, regardless of whether the first instruction is cancelled.

41. (Previously Presented) The processor of claim 40 wherein the processor includes logic to prevent a write portion of the first instruction from altering information held in at least a portion of the resource if the first instruction is cancelled.

42. (Previously Presented) A processor adapted to:

speculatively dispatch a load operation to a cache unit;

determine, following said speculative dispatch, whether read-after-write hazards associated with the load operation are present based on information in a read-after-write hazard field in a load buffer for said load

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operation wherein each bit in said read-after-write hazard field corresponds to an entry in a store buffer; and

handle a datum from the cache unit for the speculatively dispatched load operation based, at least in part, on the determining.

43. (Previously Presented) The processor of claim 42 wherein the processor is adapted to lock a resource associated with the load operation concurrently with dispatching the load operation.

44. (Previously Presented) The processor of claim 43 wherein the processor is further adapted to unlock the resource associated with the load operation no later than a time at which an instruction implementing the load operation exits an instruction pipeline, regardless of whether the instruction is cancelled before exiting the instruction pipeline.

45. (Previously Presented) A processor comprising:

means for determining whether a read-after-write hazard exists between an access to a resource to be performed by a first instruction upon execution of said first instruction in a pipeline and execution of a second instruction based, at least in part, on order of the first instruction with respect to the second instruction as indicated in a read-after-write hazard field for said first instruction in a buffer of a load/store unit of said processor wherein each bit in said read-after-write hazard field corresponds to an entry in a store buffer; and

means for locking the resource prior to said means for determining determining whether the read-after-write hazard exists.

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46. (Previously Presented) The processor of claim 45 wherein the locking means includes means for locking the resource prior to the first instruction entering a trap stage of said pipeline.

47. (Previously Presented) The processor of claim 45 wherein the first instruction is an atomic instruction including a portion to lock the resource and a portion to unlock the resource.

48. (Cancelled)

49. (Previously Presented) The processor of claim 45 wherein the locking means includes:

means for locking the resource during an effective address calculation stage of said pipeline.

50. (Previously Presented) The processor of claim 45 wherein the locking means includes means for locking at least a portion of a cache.

51. (Previously Presented) The processor of claim 45 wherein the locking means includes means for locking at least one memory address.

52. (Previously Presented) The processor of claim 45 further comprising means for unlocking the resource no later than a time at which the first instruction exits said pipeline, regardless of whether the first instruction is cancelled.

53. (Previously Presented) The processor of claim 52 wherein the unlocking means includes:

means for unlocking the resource in the normal course of executing the first instruction.

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54. (Previously Presented) The processor of claim 52 wherein the unlocking means includes:

means for preventing a write portion of the first instruction from altering information held in at least a portion of the resource.

55. (Previously Presented) The processor of claim 54 wherein the preventing means includes means for suppressing writing of a value to an architectural storage location.

56. (Previously Presented) A method of locking a resource in a processor, the method comprising:

dispatching for speculative execution a load operation prior to determining whether a read-after-write hazard exists between the load operation and a store operation indicated in a read-after-write hazard field in a load buffer wherein each bit in said read-after-write hazard field corresponds to an entry in a store buffer;

locking a resource of the load operation incident with execution of the load operation;

determining whether the read-after-write hazard exists based on information in said read-after-write hazard field in said load buffer for said load operation; and

handling a datum returned for the load operation based, at least in part, on the determining.

57. (Previously Presented) The method of claim 56 further comprising discarding the datum if it is determined the read-after-write hazard exists.

58. (Previously Presented) The method of claim 56 further comprising unlocking the resource after the datum is returned.

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